# Controllable Electrical Properties of Metal-Doped In$_2$O$_3$ Nanowires for High-Performance Enhancement-Mode Transistors

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ABSTRACT In recent years, In$_2$O$_3$ nanowires (NWs) have been widely explored in many technological areas due to their excellent electrical and optical properties; however, most of these devices are based on In$_2$O$_3$ NW field-effect transistors (FETs) operating in the depletion mode, which induces relatively higher power consumption and fancier circuit integration design. Here, n-type enhancement-mode In$_2$O$_3$ NW FETs are successfully fabricated by doping different metal elements (Mg, Al, and Ga) in the NW channels. Importantly, the resulting threshold voltage can be effectively modulated through varying the metal (Mg, Ga, and Al) content in the NWs. A series of scaling effects in the mobility, transconductance, threshold voltage, and source−drain current with respect to the device channel length are also observed. Specifically, a small gate delay time (0.01 ns) and high on-current density (0.9 mA/μm) are obtained at 300 nm channel length. Furthermore, Mg-doped In$_2$O$_3$ NWs are then employed to fabricate NW parallel array FETs with a high saturation current (0.5 mA), on/off ratio (>10^9), and field-effect mobility (110 cm^2/V·s), while the subthreshold slope and threshold voltage do not show any significant changes. All of these results indicate the great potency for metal-doped In$_2$O$_3$ NWs used in the low-power, high-performance thin-film transistors.
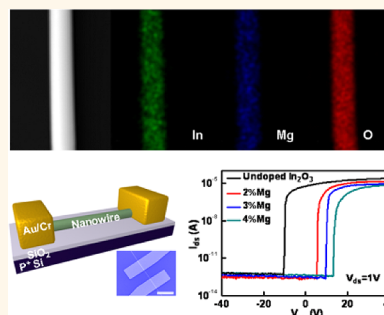
KEYWORDS: In$_2$O$_3$ nanowires · field-effect transistors · enhancement-mode · controllable threshold voltage · doping

I n the past few years, due to exceptional physical properties, semiconductor nanowires (NWs) have been widely studied and explored as fundamental building blocks for various technological applications.[1−5] Among many NW materials, metal oxide NWs such as In$_2$O$_3$ is a promising candidate for active device materials in next-generation electronics,[6−8] memory devices,[9,10] displays,[11,12] and chemical and biosensors[13−16] because of their chemical stability, wide band gap (∼3.6 eV), optical transparency, and high field-effect carrier mobility (μ_{FE}). However, most of these In$_2$O$_3$ NW field-effect transistors (FETs) operate in the n-type accumulation or depletion mode (D-mode) which exhibits nonzero current at zero gate bias and negative threshold voltage (V_{th}). These D-mode devices are beneficial for quantitative and scalable sensing applications since

the signals come from the modulation of the channel rather than the contacts,[17−19] but in the area of electronic circuits, both D-mode and enhancement mode (E-mode) devices are needed.[20−24] E-mode FETs typically operate with off-current at zero gate bias and positive V_{th}. They are more preferable to their D-mode counterparts as there is no need to utilize a gate voltage to switch off the E-mode devices such that the power consumption is relatively lower, circuit design is simpler for integration, and the transport of charge carriers can be accurately modulated by the gate structure.[20] Although the E-mode NW FETs reveal more unique advantages, it is still a big challenge to control these device operations (D-mode *versus* E-mode) with the detailed electrical characterization performed. For example, Lee *et al.* have architected the surface of ZnO NWs to modify the fabricated
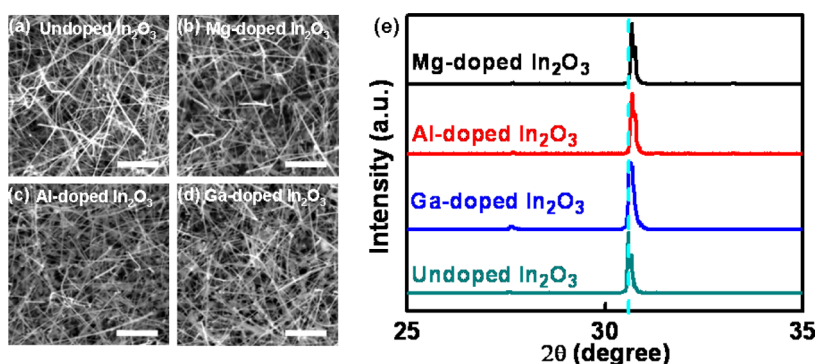
Figure 1. SEM images of (a) undoped In_2O_3, (b) Mg−In_2O_3, (c) Al-doped In_2O_3, (d) Ga-doped In_2O_3 NWs grown on a (100) silicon substrate coated with 1 nm thick Au film. The scale bars are 2 μm. (e) XRD patterns of the as-synthesized NWs.

transistor characteristics with the smooth NWs for the D-mode device operation and corrugated NWs for the E-mode FETs.[23] Also, Zhou *et al.* have explored the different surface passivation schemes in order to control the electrical properties such as V_{th} of the In_2O_3 NW devices.[25] All of these approaches have heavily relied on the modulation of surface and/or interface states of the metal oxide NW surfaces to alter their corresponding electronic transport properties, in which this NW surface modulation may be difficult for the large-scale integration due to the wire-to-wire variation in their surfaces.

In this paper, instead of controlling the surface properties, we present a simple technique to achieve n-type E-mode In_2O_3 NW FETs by simply doping different metal elements (Mg, Ga, and Al) during the NW synthesis. The resulting device threshold voltage (V_{th}) can be effectively modulated by adjusting the metal (Mg, Ga, and Al) content in the NWs with negligible changes in other electrical properties such as μ_{FE}, subthreshold slope (SS), and saturation current (I_{on}). Furthermore, electron beam lithography (EBL) technique is used to study the device scaling of Mg-doped In_2O_3 NW FETs, and a series of scaling effects are observed when the channel length is reduced. High-performance E-mode Mg-doped In_2O_3 NW parallel array devices are also fabricated, which further illustrates the technological potency of metal-doped In_2O_3 NWs for the next-generation low-power thin-film transistors (TFTs).

RESULTS AND DISCUSSION

The typical scanning electron microscopy (SEM) images of undoped, Mg-, Al-, and Ga-doped In_2O_3 NWs are shown in Figure 1a−d, respectively. It is clear that the NW morphology is not evidently affected by the doping process. All NWs are grown with diameters of 40−70 nm and lengths of tens to hundreds of micrometers. In order to confirm the metal dopant incorporation within the NW crystal structure, X-ray diffraction (XRD) is performed. Figure 1e displays the XRD spectra taken from undoped, Mg-, Al-, and Ga-doped In_2O_3 NWs. The strongest (222) peak indicates that all grown In_2O_3 NWs consist of the cubic crystal

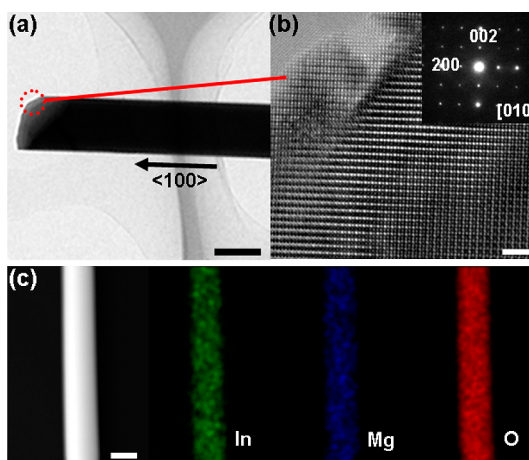**Figure 2.** (a) TEM image of a typical Mg-doped In_2O_3 NW. The scale bar is 100 nm. (b) Corresponding HRTEM image taken from the circled area in (a). The scale bar is 1 nm. (Inset) SAED pattern of the same NW, illustrating a cubic crystal structure with the ⟨100⟩ growth direction. (c) High-angle annular dark-field image of the Mg-doped In_2O_3 NW and the corresponding EDS elemental mapping. The scale bar is 50 nm.

structure in both doped and undoped samples. Although the dopants do not modify the NW crystal structure in this study, they induce the distortion of crystal lattice as evidenced by the shift of (222) peaks. This shift toward the higher angle reveals a narrowing of the lattice constant, which can be attributed to the metal ion (Ga^{3+}, Al^{3+}, Mg^{2+}) substitution in In sites of the lattice since all metal ions here have a smaller ionic radius than the one of In^{3+}.[26]

To further characterize the metal-doped In_2O_3 NWs, Mg-doped In_2O_3 NWs are studied by the high-resolution transmission electron microscopy (HRTEM) in details. As depicted in Figure 2a, the typical NW appears relatively homogeneous without any significant domain boundaries, indicating the single-crystalline nature. The HRTEM image (Figure 2b) and corresponding selected area electron diffraction (SAED) pattern (top inset, Figure 2b) further illustrate its cubic crystal structure. In addition, indexing the SAED pattern demonstrates the ⟨100⟩ direction being the NW growth direction. All
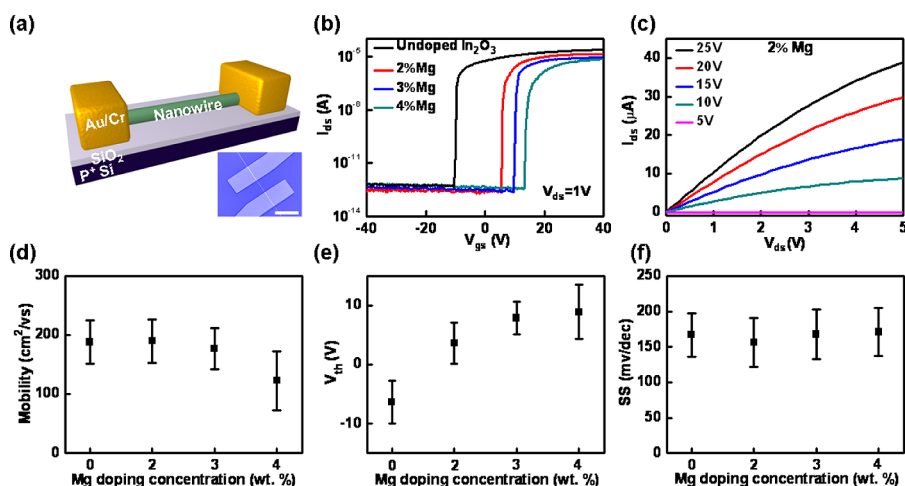
Figure 3. Electrical properties of back-gated Mg-doped In_2O_3 NW FETs fabricated on the silicon substrate. (a) Schematic and (inset) SEM image of a representative single NW FET fabricated with Cr/Au (20 nm/40 nm) electrodes and heavily doped silicon substrates covered with 110 nm thick thermally grown SiO_2. The scale bar is 5 μm. (b) I_{ds} versus V_{gs} curves at V_{ds} = 1 V for the back-gated FET with different Mg doping concentration (0, 2, 3, and 4 wt %). (c) Family of $I_{ds}-V_{ds}$ curves for the 2 wt % Mg doping concentration with V_{gs} = 25 to 5 V in -5 V steps from top to bottom. The average (d) μ_{FE}, (e) V_{th}, and (f) SS values of 15 NW devices versus Mg doping concentration.

of these results are consistent with the former study on undoped In_2O_3 NWs.[27] The energy-dispersive X-ray spectrometry (EDS) is also performed to exhibit the homogeneous distribution of In, Mg, and O atoms along the NW body (Figure 2c), which suggests uniform chemical composition along the NW axial direction.

In addition to the crystal structure, to shed light on the investigation of the electrical properties of In_2O_3 NWs with different Mg doping concentration, NW FETs (Figure 3) are fabricated with different NW channels grown with various weight ratios of MgO powder in the source materials, which are set to 10:0.5:2, 10:1:2, and 10:2:2 (In_2O_3/MgO/graphite). The corresponding Mg content of the grown NWs is then assessed by EDS, and the doping concentration (weight ratio) is estimated to be ~2, 3, and 4 wt %, respectively. The devices are measured at a fixed condition including temperature, humidity, and V_{gs} sweep rate so as to avoid the disturbance of uncertainty random circumstance factor. The hysteresis of $I_{ds}-V_{gs}$ is observed when V_{gs} is swept from -40 V to $+40$ V and back to -40 V; however, the hysteresis does not show significant difference for these devices (see Supporting Information Figure S1). Figure 3b shows the representative I_{ds} versus V_{gs} curves for different Mg doping concentration, and they all exhibit the standard n-type transistor behavior as expected. The threshold voltages, V_{th} (confirmed from the horizontal intercept of a linear part in $I_{ds}^{1/2}$ vs V_{gs} plot), are -10, 5.6, 10, and 13.6 V for the Mg doping concentration of 0, 2, 3, and 4 wt %, accordingly, producing a remarkable shift to more positive voltages with the increasing Mg concentration. This shift indicates that the D-mode In_2O_3 NW FETs are successfully transformed into the E-mode when the Mg doping is increased. Figure 3c depicts the output characteristics recorded from the same device (2 wt % Mg), showing

that I_{ds} increases linearly with V_{ds} at low V_{ds} and saturates at high V_{ds}. The linear regime can be attributed to the good ohmic contacts between the Cr/Au electrodes and the NWs. The pinch-off and I_{ds} saturation suggest that the carrier transport is completely controlled by the gate bias.

Moreover, a statistical analysis to correlate the changes in μ_{FE}, V_{th} and SS to the Mg doping concentration is also performed. The average and standard deviation for these quantities are calculated based on 15 NW FETs for each type. The μ_{FE} is estimated using the equation

$$\mu_{FE} = \frac{g_m L^2}{C_g V_{ds}} \tag{1}$$

in the linear operation regime. Here $g_m = dI_{ds}/dV_{gs}$ is the transconductance, and $L = 3$ μm is the nanowire device channel length. C_g is the capacitance of the back gate which can be estimated by utilizing the cylinder on-plane model:

$$C_g = \frac{2\pi\varepsilon_0\varepsilon_r L}{\ln(4h/d)} \tag{2}$$

where ε_0 is the permittivity of free space, ε_r is the dielectric constant of SiO_2, $h = 110$ nm is the thickness of the SiO_2 layer that is measured by ellipsometry, and d (50 $\pm$ 15 nm) is the NW diameter. Using the estimated capacitance values and measured device parameters, the average μ_{FE} values are estimated to be 188, 190, 177, and 123 $cm^2/V\cdot s$ for the Mg doping concentration of 0, 2, 3, and 4 wt %, respectively (Figure 3d). Considering the enhanced ionized impurity scattering for the increased Mg doping, this mobility degradation is expected but not significant. Then the average V_{th} value also changes from -6.4 to 8.9 V as the Mg concentration increases (Figure 3e); this positive shift is believed to be associated with the reduced carrier concentration (n), which can be
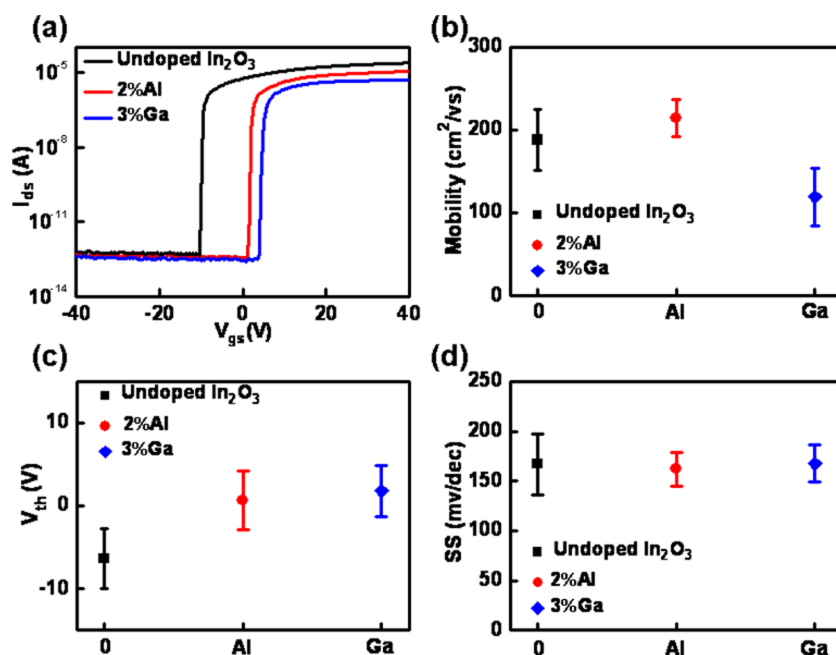
Figure 4. (a) I_{ds} vs V_{gs} curves at $V_{ds} = 1$ V for the undoped, Al-doped, and Ga-doped In_2O_3 NW FETs. Average (b) μ_{FE}, (c) V_{th}, and (d) SS values of 15 FETs fabricated with undoped, Al-doped, and Ga-doped In_2O_3 NWs as the device channels.

estimated by this equation:

$$n = \frac{4C_g(V_{gs} - V_{th})}{\pi q d^2 L} \quad (3)$$

Here, q is the electronic charge. At $V_{gs} = 20$ V, the average values of n are ~6.4×10^{18} cm^{-3} for undoped In_2O_3, ~4.0×10^{18} cm^{-3} for 2 wt % Mg, ~2.9×10^{18} cm^{-3} for 3 wt % Mg, and ~2.7×10^{18} cm^{-3} for 4 wt % Mg. This degradation of carrier concentration is possibly due to the compensation of the oxygen vacancies by the acceptor Mg.[28−30] Meanwhile, the reduced carrier concentration and μ_{FE} also lead to the slight decrease of I_{on}. In view of the standard deviation, the SS value does not show any significant change (Figure 3f), indicating that the Mg doping has little affection for the interfacial trap density here.[1] Moreover, all of these devices show an extraordinary on/off current ratio (>10^7), exhibiting excellent semiconducting characteristics for device applications.

At the same time, Al and Ga doping are also performed in the In_2O_3 NW synthesis in order to evaluate their doping effect on the NW device characteristics. This way, the NWs are grown with the same weight ratio of the source material (In_2O_3/Al_2O_3 or $Ga_2O_3/$ graphite = 10:1:2) for each case. On the basis of the EDS analysis, the Al and Ga doping concentration is estimated to be 2 and 3 wt %, respectively. Figure 4a gives the representative I_{ds} versus V_{gs} curves for the undoped, Al-doped, and Ga-doped In_2O_3 NW FETs. Similar to the one of Mg doping, these devices exhibit a standard n-type FET behavior with a positive voltage shift in V_{th}. The average and standard deviations for μ_{FE}, V_{th}, and SS values calculated based on 15 FETs are

shown in Figure 4b−d, accordingly. Compared to the Ga doping, the Al-doped In_2O_3 NW FET has slightly better electrical performance in μ_{FE} and saturation current, which can be attributed to the difference in the carrier scattering and electron concentration caused by these two different impurity ions. Notably, the SS values depicted in Figure 4d are all very similar with the undoped case, indicating that small amounts of Al^{3+} or Ga^{3+} have an inferior effect on the interfacial trap density, as well. In the future studies, when the doping concentration is further increased, a more effective control over V_{th} can also be expected.

To demonstrate the potency of these metal-doped In_2O_3 NWs for the scaled transistors, the dependence of device electrical properties on the channel length is studied. The FET used in this study is fabricated by EBL with the Mg-doped In_2O_3 NW channel (3 wt % Mg; diameter of 53 nm). Figure 5a presents the corresponding I_{ds}−V_{gs} curves for different channel lengths (0.3, 0.5, 0.8, 1.5, and 3 μm) at a fixed drain bias of 1 V with the inset showing the device SEM image. It can be clearly seen that the device exhibits standard n-type E-mode FET behaviors, even though the channel length is decreased to 0.3 μm. Because the off-current (~10^{-13} A) is maintained at the similar value and oncurrent increases with the reduced channel length, a large on/off current ratio (>10^8) is achieved at $L = 0.3$ μm. The changes in other typical electrical characteristics (μ_{FE}, g_m, V_{th}, and on-current) are also illustrated in Figure 5b,c. As the channel length is decreased, the V_{th} shifts from 10.8 V ($L = 3$ μm) to 8 V ($L = 0.3$ μm), and this negative shift can be well explained by the charge-sharing model. According to this model, when
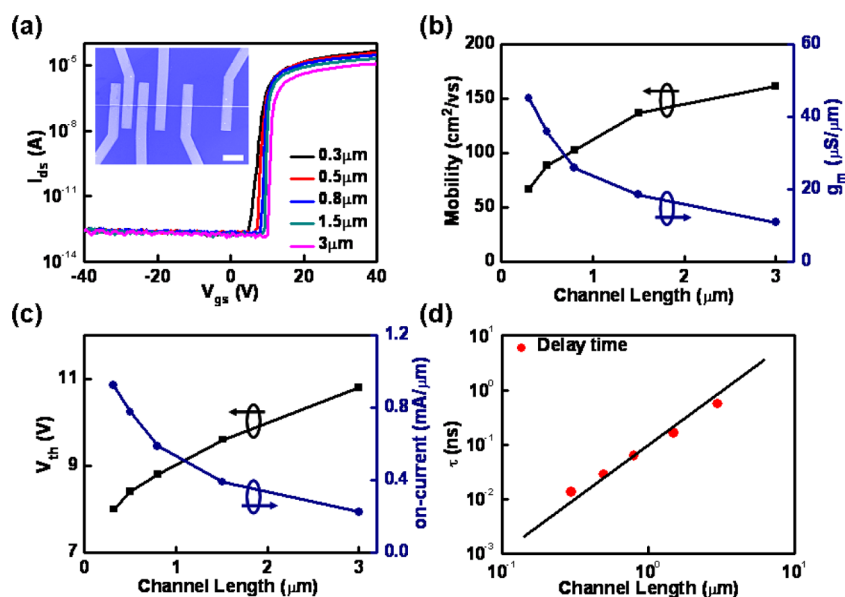
Figure 5. (a) I_{ds} vs V_{gs} curves for various channel lengths at fixed V_{ds} = 1 V. The inset is the SEM image of the device that was fabricated by EBL with the Mg-doped In_2O_3 NW channel. The scale bar is 2 μm. (b) Plots of μ_{FE} and g_m vs channel length. (c) Plots of V_{th} and on-current (at V_{ds} = 1 V and V_{gs} = 40 V) vs channel length. (d) Plots of intrinsic delay τ vs channel length. The solid linear line is a fit to the data point.

the channel is scaled, the effective channel length would reduce since the charges that are depleted by the source and drain junctions cannot be neglected for shorter channel; as a result, the V_{th} value that used to create a charge accumulation in the channel would also get decreased.[31] In addition, assuming the effective channel width equals the NW diameter, due to the reduced channel resistance, a larger g_m (45.1 μS/μm) and on-current (0.9 mA/μm, under V_{ds} = 1 V and V_{gs} = 40 V) can be obtained, as well, at L = 0.3 μm. Importantly, this current density is comparable to that of the state-of-the-art Si MOSFETs ($\sim$1 mA/μm). On the other hand, Figure 5b shows that μ_{FE} is decreased gradually with reduced channel length. This is probably because the parasitic contact resistance cannot be neglected in shorter channel FETs; otherwise, the short channel length here may become comparable to the mean free path of charge carriers and lead to the quasi-ballistic transport.[31,32] Another important parameter, the intrinsic gate delay time (τ) which provides a frequency limitation for the transistor operation,[33] is also discussed here. It is calculated by this equation:

$$\tau = \frac{C_g}{g_m} = \frac{L^2}{\mu_{eff} V_{ds}} \quad (4)$$

As shown in Figure 5d, the values of τ decrease from 0.56 ns (L = 3 μm) to 0.01 ns (L = 0.3 μm); the resulting formations of the devices are fit with L^2. According to the projected cutoff frequency (f_T) equation

$$f_T = \frac{1}{2\pi\tau} \quad (5)$$

the value of f_T can be as large as up to 16 GHz at V_{ds} = 1 V, indicating that Mg-doped In_2O_3 NW FETs have

great potency for high-speed devices with the low power consumption.

Also, a Mg-doped In_2O_3 NW (3 wt % Mg) parallel array FET is then fabricated to prove the feasibility of large-scale integration of these NWs for TFT applications. Figure 6a shows the optical image and schematic of the device, while Figure 6b gives the corresponding $I_{ds}-V_{gs}$ curves, exhibiting a typical n-type E-mode FET behavior as expected. Under V_{ds} = 5 V and V_{gs} = 40 V, it achieves a saturation current of 0.5 mA and a large on/off current ratio ($>10^9$). Furthermore, the μ_{FE} value at V_{ds} = 1 V can be estimated with the equation[34]

$$\mu_{FE} = \frac{g_m L^2}{N C_g V_{ds}} \quad (6)$$

Here, N = 20 is the number of NWs contained in the channel. On the basis of this equation, the peak mobility is estimated to be $\sim$110 $cm^2/V\cdot s$ (Figure 6b inset). This mobility value is on the same level of that of state-of-the-art semiconductor carbon nanotube networks, which is calculated using the same cylinder-on-the-plane model.[35] Moreover, the SS value is $\sim$148 mV/dec, and V_{th} is $\sim$8.8 V, which are similar to those of the single NW FET. Notably, as compared to the single NW FET, the average current of each NW reduces slightly. This can be attributed to the increased parasitic capacitance that is caused by the misaligned and broken NWs in the channel.[36] I_{ds} versus V_{ds} relation at various V_{gs} values is also shown in Figure 6c, indicating that the carrier transport in the channel can be completely controlled by the gate bias since I_{ds} increases linearly with V_{ds} and saturates at higher V_{ds}. All of these results suggest that Mg-doped In_2O_3 NW parallel array FETs can be used for high-performance E-mode TFTs. In the
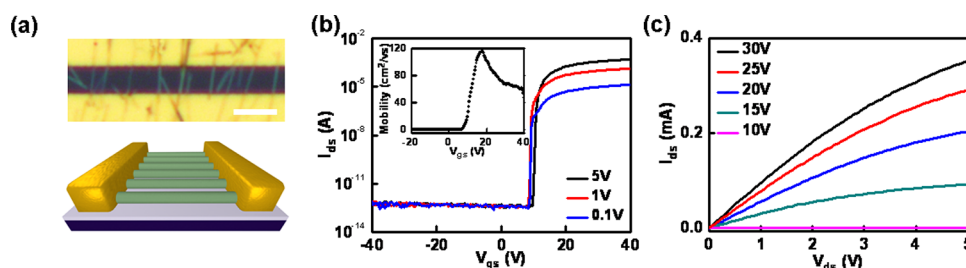
Figure 6. Electrical characteristics of the Mg-doped In_2O_3 NW (3 wt % Mg) parallel array FET. (a) (Top) optical and (bottom) schematic of a back-gated Mg-doped NW array FET. The scale bar is 5 μm. (b) $I_{ds}-V_{gs}$ curves at V_{ds} = 0.1, 1, and 5 V, respectively, and about 20 NWs bridging source/drain. (Inset) Mobility assessment of this NW array device under V_{ds} = 1 V. (c) $I_{ds}-V_{ds}$ curves with V_{gs} = 30 to 10 V in −5 V steps from top to bottom.

future, further improvement of the device performance could be expected by optimizing the NW density, reducing channel length, and using a top-gated structure with high-k dielectrics.

CONCLUSIONS

In summary, n-type enhancement-mode In_2O_3 NW FETs are successfully fabricated by doping different metal elements (Mg, Ga, and Al) in the NW channels, which show adjustable threshold voltage with different doping concentration without affecting device characteristics much. Meanwhile, when the channel length is reduced, a series of scaling effects are observed for the Mg-doped In_2O_3 NW FETs such as the shorter delay time down to 0.01 ns. Furthermore, Mg-doped In_2O_3 NWs are also employed to fabricate n-type E-mode NW parallel array FETs, and impressive saturation current (0.5 mA), on/off ratio ($>10^9$) and mobility (110 $cm^2/V\cdot s$) are obtained, indicating the great potency of Mg-doped In_2O_3 NWs for low-power, high-performance TFTs.

METHODS

Nanowire Synthesis. The metal-doped In_2O_3 NWs used in this study were synthesized in a horizontal tube furnace utilizing a simple chemical vapor deposition (CVD) method. A mixture of doping metallic oxide powder, In_2O_3 powder, and graphite powder with the weight ratio of 10:1:2 was placed into a quartz boat, and silicon substrates coated with 1 nm of gold catalyst were then placed in the downstream position about 10 cm away from the evaporation source. Then, the whole setup was inserted into a quartz tube reactor. The source and substrate were heated to 1100 and 900 °C, respectively, and kept at this temperature for 1 h under a constant flow of gas (argon/oxygen = 100:1) at a flow rate of 200 sccm. When the system had cooled to room temperature, a large amount of NWs was formed on the surface of the silicon substrate.

FET Fabrication and Characterization. After growth, the NWs were transferred to the precleaned highly doped p-type silicon substrates with a thermally grown 110 nm thick SiO_2 layer. Then the substrates were spin-coated with MMA and PMMA, and the EBL (JEOL 6510 with NPGS) was employed to define the source and drain pattern. The Cr/Au (20 nm/40 nm) electrodes were completed by metal evaporation and lift-off processes. Electrical performance of fabricated back-gated NW FETs was performed with the Lake Shore TTPX Probe Station and Agilent 4155C semiconductor parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Hysteresis characteristics of the Mg-doped In_2O_3 NW FET. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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